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10/034,138	12/27/2001	Choon-Seng Tan	P01-3977	1621

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EXAMINER	
VU, TRISHA U	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,138	TAN ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 9, 13-14, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641).

As to claim 1, Mori teaches a data array system for providing a host computer device having a host bus redundant access to a data storage device (100) (at least Fig. 1 and Fig. 7), comprising: an active controller (Control Apparatus #1) linked to the data storage device (100), the active controller including a messaging mechanism for transmitting the messages and data over a host bus (from a host device); and a standby controller (Control Apparatus #2) linked to the data storage device, the standby controller including message and data buffers for storing the messages and data (Fig. 1 and col. 6, lines 1-50). However, Mori does not explicitly disclose the active controller and the standby controller linked to the host bus whereby the host bus functions as an inter-controller-link. Herbert teaches redundant controllers that attach directly to the host system's main PCI bus (col. 4, lines 32-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the active controller

and the standby controllers both linked directly to the host PCI bus as taught by Herbert in the system of Mori to minimize the number of buses for connecting devices and thus reduce the system cost, also PCI bus provides high speed and plug and play advantages.

As to claim 2, Herbert further teaches the host bus is a peripheral component interconnect (PCI) bus (col. 4, lines 32-40).

As to claim 3, Herbert further teaches the active and the standby controllers are PCI-compliant devices (col. 4, lines 32-40).

As to claim 9, Mori teaches a method for providing communications between an active controller (Control Apparatus #1) and a standby controller (Control Apparatus #2) configured for redundant communications between a host (host device) and a storage device (100), comprising: at the active controller, building a message; with the active controller, transferring the message to the standby controller; with the active controller, writing to a command/reply queue at the standby controller (at least a command in Fig. 9); with the standby controller, checking the command/reply queue for a next message; and upon detecting the next message, processing with the standby controller the transferred message (Fig. 1, Fig. 7, and col. 6,lines 1-50). However, Mori does not explicitly disclose the active controller and the standby controller linked to the host bus whereby the host bus functions as an inter-controller-link. Herbert teaches redundant controllers that attach directly to the host system's main PCI bus (col. 4, lines 32-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the active controller and the standby controllers both linked directly to the host PCI bus as taught by Herbert in the system of Mori to minimize the number of

buses for connecting devices and thus reduce the system cost, also PCI bus provides high speed and plug and play advantages.

As to claim 13, Mori further teaches after the processing, with the standby controller writing to a reply queue at the active controller to indicate the processing is complete (a write instruction completion report is sent to the host device) (col. 6, lines 43-50).

As to claim 14, Mori teaches a data storage system with redundant data storage, comprising: a host processor (host device); an active controller (Control Apparatus #1) controlling access by the host processor to data storage devices (100); a standby controller (Control Apparatus #2) controlling access by the host processor to the data storage devices; wherein the active and standby controllers include redundancy messaging mechanisms (Fig. 1, Fig. 7, and col. 6,lines 1-50). However, Mori does not explicitly disclose a host bus communicatively linking the host processor, the active controller, and the standby controller, to assert and sample signals on the host bus to provide inter-controller communications over the host bus. Herbert teaches redundant controllers that attach directly to the host system's main PCI bus (col. 4, lines 32-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the active controller and the standby controllers both linked directly to the host PCI bus as taught by Herbert in the system of Mori to minimize the number of buses for connecting devices and thus reduce the system cost, also PCI bus provides high speed and plug and play advantages.

As to claim 17, Mori further teaches the standby controller includes a data buffer (cache memory 11') and wherein the active redundancy messaging mechanism transfers data corresponding to the message over the host bus to the data buffer (col. 7, lines 19-50).

As to claim 20, Herbert further teaches the host bus is a peripheral component interconnect (PCI) bus and the active and standby controllers are PCI-compliant devices. (col. 4, lines 32-40).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641) in view of Osman et al. (5,659,718) (hereinafter Osman).

As to claim 4, the argument above for claim 1 applies. Mori further teaches the standby controller includes a queue (cache memory 11') for storing information from the active controller over the host bus to provide processing information for the transmitted messages and data (col. 7, lines 19-62). However, Mori and Herbert not explicitly disclose the information includes a signal identifier. Osman teaches a signal identifier (at least start field 701 and end field 705 to indicate the start and the end of the frames and bursts) (col. 12, lines 31-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the signal identifier as taught by Osman in the system of Mori and Herbert so that the destination device will better process and reconstruct the information properly.

4. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641) and Osman et al. (5,659,718) (hereinafter Osman), and further in view of Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt).

As to claim 5, the argument above for claim 4 applies. However, Mori, Herbert, and Osman do not explicitly disclose processing the signal identifier in response to an interrupt from the active controller. Burkhardt teaches processing the message by the destination device (processor 22) in response to an interrupt from the source device (processor 29) after the message is copied into a buffer (Fig. 6, abstract, and col. 12, lines 34-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the interrupt as taught by Burkhardt in the system of Mori, Herbert, and Osman to notify the destination device of the existence of the message.

As to claim 6, Osman further teaches the signal identifier indicates the stored messages and data as a message-only transfer, a message-with-partial data transfer, or a message-with-data transfer (single frame or a burst).

As to claim 7, Mori further teaches the standby messaging mechanism moves data in the data buffer to memory as part of the processing of the stored messages and data (col. 12, lines 37-54).

As to claim 8, Mori further teaches the active controller includes a reply queue and the standby messaging mechanism replies to the transmitted messages and data by writing a reply message to the reply queue indicating messaging can be transmitted by the active controller (a write instruction completion report is sent to the host device) (col. 6, lines 43-50).

5. Claims 10-11 and 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641), and further in view of Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt).

As to claim 10, the argument above for claim 9 applies. However, Mori and Herbert do not explicitly disclose driving an interrupt with the active controller to standby controller and wherein the checking is performed in response to the standby controller sampling the interrupt. Burkhardt teaches processing the message by the destination device (processor 22) in response to an interrupt from the source device (processor 29) after the message is copied into a buffer (Fig. 6, abstract, and col. 12, lines 34-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the interrupt as taught by Burkhardt in the system of Mori and Herbert to notify the destination device of the existence of the message.

As to claim 11, Mori further teaches transferring data with the message, and wherein the transferred message indicates a presence or absence of the data (at least Fig. 9).

As to claims 18-19, the argument above for claim 17 applies. Mori further teaches the standby redundancy messaging mechanism transfers the data from the data buffer to another memory device to enable receipt of additional data (at least col. 12, lines 37-54). However, Mori and Herbert do not explicitly disclose transmitting a signal to the active controller upon completion of the transfer of the data out of the data buffer and transmitting an interrupt to the active controller. Burkhardt teaches transmitting a

signal (response available) to the source device (processor 29) upon completion of the transfer of the data out of the data buffer and transmitting an interrupt to the source device (col. 14, lines 57-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide completion notification and interrupt to the source device as taught by Burkhardt in the system of Mori and Herbert to notify/update the source device of the processing status.

6. Claims12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641) and Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt), and further in view of Osman et al. (5,659,718) (hereinafter Osman).

As to claim 12, the argument above for claim 11 applies. Mori, Herbert, and Burkhardt not explicitly disclose the message defines the data as all or partial and wherein the standby controller stores the data based on the all or partial data definition. Osman teaches message including information which defines the data as all or partial (a frame or a burst) (col. 12, lines 31-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include information which defines the data as all or partial as taught by Osman in the system of Mori, Herbert, and Burkhardt so that the destination device will better process and reconstruct the information properly.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641), and further in view of Hayashi et al. (6,115,803) (hereinafter Hayashi).

As to claim 15, the argument above for claim 14 applies. However, Mori further teaches the standby controller includes a message buffer for storing messages (cache memory 11') wherein the active redundancy mechanism transfers messages to the message buffer of the standby controller (Fig. 1, Fig. 7, and col. 6, lines 43-50). However, Mori and Herbert not explicitly disclose the standby controller includes a command/reply queue for registering receipt of new messages, and wherein the active redundancy mechanism writes to the command/reply queue to indicate the transmittal of the messages. Hayashi teaches command/reply queue for registering the messages (at least col. 6, lines 14-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include command/reply queue as taught by Hayashi in the system of Mori and Herbert to keep track of the command processing.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641) and Hayashi et al. (6,115,803) (hereinafter Hayashi), and further in view of Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt).

As to claim 16, the argument above for claim 15 applies. However, Mori, Herbert, and Hayashi not explicitly disclose the active redundancy mechanism asserts an interrupt to the standby controller over the host bus and the standby redundancy mechanism responds to the interrupt by checking the command/reply queue. Burkhardt

teaches asserting an interrupt to the destination device (processor 22) for checking its command queue (126) (Fig. 6, abstract, and col. 12, lines 34-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the interrupt as taught by Burkhardt in the system of Mori, Herbert, and Hayashi to notify the destination device of the existence of the message.

9. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (6,606,683) in view of Herbert (6,151,641), and further in view of Iswandhi et al. (5,675,807) (hereinafter Iswandhi).

As to claim 21 Mori teaches a method for providing inter-controller communications between an active controller (Control Apparatus #1) and a standby controller (Control Apparatus #2) configured for redundant communications between a host (host device) and a storage device (100) (Fig. 1, Fig. 7, and col. 6, lines 1-50). However, Mori does not explicitly disclose the active controller and the standby controller linked to a host bus. Herbert teaches redundant controllers that attach directly to the host system's main PCI bus (col. 4, lines 32-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the active controller and the standby controllers both linked directly to the host PCI bus as taught by Herbert in the system of Mori to minimize the number of buses for connecting devices and thus reduce the system cost, also PCI bus provides high speed and plug and play advantages. However, Mori and Herbert do not explicitly disclose specifying a range of memory in the standby controller as an interrupt range; writing data to the interrupt range

of the standby controller by the active controller; and driving a local interrupt at the standby controller. Iswandhi teaches specifying a range of memory in the destination device as an interrupt range; writing data (packetized message) to the interrupt range of the destination device by the source device; and driving a local interrupt at the standby controller (storage of the interrupt data will initiate an internal interrupt to notify the destination device) (at least abstract and col. 6 line 61 to col. 7 line 16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interrupt message delivery as taught by Iswandhi in the system of Mori and Herbert to notify the destination of an event wherein the system can minimize the requirement of additional interrupt lines.

As to claim 22, Iswandhi further teaches the interrupt driving is performed with a memory controller (BTE 88) in the standby controller (destination CPU) (Fig. 5 and col. 16, lines 37-51).

As to claim 23, Mori further teaches writing to a reply queue at the active controller by the standby controller (a write instruction completion report is sent to the host device) (col. 6, lines 43-50).

Response to Arguments

10. Applicant's arguments filed 07-19-04 have been fully considered but they are not persuasive:

With respect to Applicant's argument on page 12 of the Remarks that "Herbert does not teach or suggest active and standby controllers linked to a host bus which

functions as an inter-controller-link", it is noted that Mori already taught active and standby controllers. However, Mori does not explicitly disclose a host bus which functions as an inter-controller-link to which the active and standby controllers linked. Therefore, Herbert reference was brought in to show a host bus which functions as inter-controller-link.

Applicant further stated that "the Office fails to provide any evidence that such a system would be less costly" (page 13 of the Remarks), note that Mori does not explicitly disclose the how the active and standby controllers linked to the host bus, therefore they could directly linked to the host bus or indirectly linked to host bus which can be through several buses before it reaches the host bus. Herbert teaches RAID controllers that attach directly to the host bus (col. 4, lines 32-40), therefore reducing the number of buses for connecting devices and thus reduce the system cost. The second advantage is the host PCI bus provides high speed and plug and play features.

With respect to Applicant's argument on pages 14-15 of the Remarks that "The art of record contains no evidence that such a combined system would allow the host bus to act as the inter-controller-link", it is noted that Herbert teaches host bus (PCI) which acts as the inter-controller-link between controllers. Applicant has not addressed in the claims how the inter-controller-link host bus works or how it is different from the PCI host bus in Herbert.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
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Sumati Lefkowitz

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PRIMARY EXAMINER